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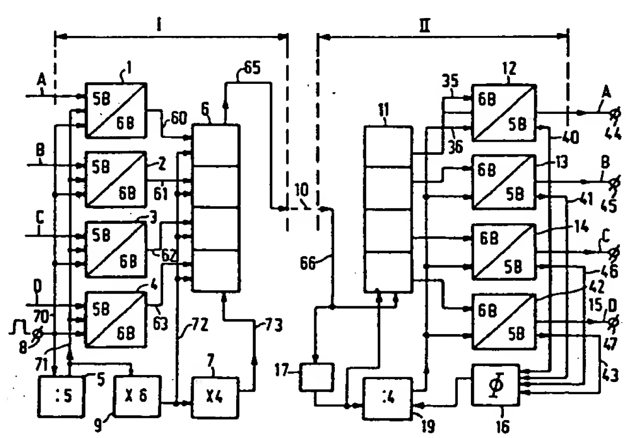
(54) Higher order digital transmission system including a multiplexer and a demultiplexer.

(57) Higher order digital transmission system including a multiplexer having N parallel inputs to which tributary input signal streams are applied, and a demultiplexer having N parallel outputs from which the tributary signal streams are taken. The signal processing operations, such as scrambling, justifying, line coding, error monitoring and word synchronization are effected before the multiplexer and after the demultiplexer.



EP 0 206 409 A1

Higher order digital transmission system including a multiplexer and a demultiplexer.

The invention relates to a higher order digital transmission system including a digital multiplexer having N parallel inputs, and a digital demultiplexer having N parallel outputs for transmitting N mutually synchronized digital signal streams through a common digital path between said multiplexer and demultiplexer, where $N \geqslant 2$ and the multiplexer being arranged for cyclically and symbol-sequential interleaving the N digital signal streams to form a composite digital signal stream, the transmission system further including at least a block coding arrangement and a block decoding arrangement.

In a digital multiplexer, N incoming signal streams (tributaries) are combined to form one outgoing signal stream, whilst the opposite operation occurs in the demultiplexer. Multiplexing the incoming signal streams is effected by means of interleaving, which implies that a bit from a binary signal stream 1 is followed by a bit from a binary signal stream 2 etc. The resultant outgoing signal stream has a digital rate which is higher than or equal to N times the digital rate of the N incoming signal streams. This is caused by the fact that the outgoing signal stream requires its own frame word and a few service bits, which are added to the outgoing signal stream. Provisions are also taken to compensate for frequency differences between the tributary signal streams and the multiplex clock. This is necessary since each of the tributary signals has its own free-running clock frequency. To this end, idle bits are injected into the multiplex signal, together with control bits, which indicate the status of the idle bits. This process is called positive justification and in general is the simplest manner of multiplexing pleisiochronous signal streams.

When digital signals are conveyed over long distances it is customary to use a form of encoding in the transmitter portion and a form of decoding in the receiver portion of the transmission system, such that the digital signal is adapted to the digital path. This digital path may, for example, be constituted by symmetrical or coaxial cables, optical fibres or the air. One of the objects usually is the suppression of the direct current component, which permits of the use of alternating current couplings in the transmission system, and direct current supply of the regenerators from the transmission system _via_ the transmission cable being possible. Another object often is to increase the pulse density of the digital signal to be conveyed, or to ensure a minimum pulse density such that recovering a clock signal, required in regenerative circuits, is possible.

In a blocking coding arrangement use is made of what are commonly referred to as code translation Tables, such as the Tables described in, for example, Philips Telecommunication Review, vol. 34, no. 2, June 1976, pages 72-86. A series/parallel converter which divides the bit stream applied to its input in consecutive blocks of a predetermined number of bits n is provided at the input of the encoding arrangement. A block of n bits is thereafter converted with the aid of the translation code matrix into a new block of m symbols in accordance with a specific instruction. Blocks of m symbols are reconverted at the output of the encoding arrangement with the aid of a parallel/series converter into a bit stream which is conveyed to the receiver portion of the digital transmission system _via_ the digital path (cable, optical fibre). In the receiver portion of the system, the bit stream applied there is subjected to a reverse process with the aid of the decoding arrangement. Examples of an encoding arrangement and a decoding arrangement are described in, for example, Proceedings 17th International Scientific Congress on Electronics, Rome, 16-18 March 1970, pages 275-283.

A higher order digital multiplex system of the above-defined type is disclosed in, for example, C.C.I.T.T. Recommendation G922. In this disclosure the frame structure of a multiplex system having 4 tributary signal streams of 140 Mbit/s each is described. A frame has a length of 2688 bits and comprises: a 12-bit frame synchronizing word; 4 service bits; 4 5-bit justification control words, one for each tributary signal stream; 4 justifiable bits, one for each tributary signal stream and 2648 time slots for the information from the four tributary signal streams. The block encoding arrangement is arranged subsequent to the multiplexer and the block encoding arrangement precedes the demultiplexer. This results in it being necessary that both the block encoding arrangement and the block decoding arrangement must be operated at the full line rate. When this line rate increases to above 565 Mbit/s, realizing the encoding and decoding arrangements becomes problematical, as low-dissipation digital modules are required. In the present state of the art of the industrial integration processes it is not possible to realize these modules, or it is very difficult to do so. Consequently, it is very difficult to apply in a higher order digital transmission system the same design philosophies customary for a lower order digital transmission system.

The invention has for its object to provide a novel concept of a higher order digital transmission system of the type defined in the preamble, which solves the above-mentioned problems.

The invention is characterized, in that each of the N digital signal streams is applied to one of the N parallel inputs of the multiplexer <u>via</u> a block encoding arrangement, that the N digital signal streams are entered synchronously under the control of a common clock signal into the N block encoding arrangements and, in the respective block encoding arrangements, are provided with a word synchronizing characteristic, that the parallel outputs of the demultiplexer are each connected to the

input of a block decoding arrangement, that the signals applied to the parallel outputs of the demultiplexer are entered into the respective block decoding arrangements under the control of the clock signal recovered from the composite digital signal, that the outputs of the block decoding arrangements are each connected to a signal output of the transmission system, that in a phase comparator arrangement the word synchronizing characteristics of the block decoding arrangements are compared with each other, whereafter as a function of the phase differences measured between said word synchronizing characteristics the phase of the read clock is controlled such that thereafter the block decoding arrangements display the word synchronizing characteristics with the mutual phase differences produced at the transmitter end.

The invention will now be described in greater detail by way of example with reference to the accompanying drawing.

Figure 1 shows a higher order digital transmission system according to the invention;

Figure 2 shows a time-sequence diagram of the multiplexer;

Figure 3 shows time-sequence diagrams of the four possible phase positions of the demultiplexer;

Figure 4 shows a time-sequence diagram of the symbols occurring at the output of the demultiplexer.

Figure 5 shows an embodiment of a block decoding arrangement.

In the higher order digital transmission system shown in Figure 1, I is the transmitter portion of the system and II the receiver portion of the system. The transmitter portion I comprises the block encoding arrangements 1, 2, 3 and 4, the multiplexer 6, the divider 5 and the multipliers 7 and 9. The receiver portion II comprises the block decoding arrangements 12, 13, 14 and 15, the demultiplexer 11, the phase comparator 16, the divider 19 and the clock regenerator 17. The N mutually synchronized digital signal streams A, B, C and D are applied to

the signal input of one of the respective block encoding arrangements 1 to 4. In the embodiment shown N=4. The write clock inputs of the block encoding arrangements 1 to 4 are together connected to the clock input 8 of the transmitter portion I of the transmission system <u>via</u> the line 70. The clock input 8 is connected <u>via</u> a divide-by-5-divider and the line 71 to the clock inputs of the block encoding arrangements 1 to 4, which from the four digital signal streams A to D form 5-bit blocks, and also to the input of a multiply-by-6 multiplier 9. The output of the multiply-by-6 multiplier 9 is connected <u>via</u> the line 72 to the write clock inputs of the multiplexer 6 and also <u>via</u> a multiply-by-4 multiplier to the read clock outputs of the multiplexer 6. Each of the signal outputs 60 to 63 of the block encoding arrangements is connected to a signal input of the multiplexer 6. The signal output 65 of the multiplexer 6 is connected <u>via</u> a digital path 10 to the input 66 of the receiver portion II of the transmission system. The input 66 is connected to the signal input of the demultiplexer 11 and also to the input of the clock regenerator 17. The output of the clock regenerator 17 is connected to the clock input of the demultiplexer 11 and also to the input of a divide-by-4 divider 19. The output of the divider 19 is connected to the write clock inputs of the block decoding arrangements 12 to 15. The original digital signal streams A to D are again available at the outputs 44 to 47 of the block decoding arrangements 12. The outputs 40 to 43 of the block decoding arrangements 12 to 15 are each connected to an input of the phase comparator 16.

Let it be assumed that the four incoming digital signals A to D are binary signals having a symbol rate (= bit rate) of 140 Mb/s. These digital streams are entered synchronously into the 5B/6B block encoding arrangements 1 to 4 with the aid of the 140 MHz clock signal present on the line 70. In the 5B/6B block encoding arrangements the 140 Mbit/s signal streams are divided by means of the 28 MHz clock signal present on the line 71 into blocks each having a length of 5 symbols. The 5-bit blocks are there-

after translated in the block encoding arrangements into blocks of 6 symbols. The block decoding arrangements 1 to 4 produce at their respective outputs 60 to 63 digital signal streams of each 6/5 x 140 = 168 Mbaud. The four digital signal streams supplied from the outputs 60 to 63 of the block encoding arrangements 1 to 4 are entered in parallel into the multiplexer 6 with the aid of the clock signal produced by the multiplier 9 and having a frequency of 6 x 28 = 168 MHz. Using the clock signal present at the output of the multiplier 7, which signal has a digital rate of 4 x 168 = 672 MHz, the digital content of the multiplexer 6 is read serially.

In the four parallel 5B/6B block encoding arrangements, the 6B words are each provided with a word synchronizing characteristic. Since the four parallel 5B/6B block encoding arrangements 1 to 4 are controlled by the same 28 MHz clock signal and the block encoding arrangements 1 to 4 are identical, the 6B words will appear with the same phases at the outputs 60 to 63 of the block encoding arrangements. This is shown schematically in the time-sequence diagram of Figure 2. The word synchronizing characteristics K(1) ... K(4) shown symbolically by means of upright lines arrive at the same instant at the outputs 60 ... 63 of the block encoding arrangements. Consequently, the mutual difference between the synchronizing characteristics is equal to 0 degrees. With the aid of the 672 MHz clock signal present at the output of the multiplier 7 always 4 bits are arranged one after the other with the same indices. A composite digital signal of the shape shown in the time-sequence diagram of Figure 2 appears at the output 65 of the multiplexer 6.

The composite digital signal is applied to the input 66 of the receiver sections II of the digital transmission system via the digital path 10. Using the clock regenerator 17, the clock signal which is used for further signal processing in the receiver portion II of the transmission system is recovered from the composite digital signal. The recovered 672 MHz clock signal is applied to

the clock input of the multiplexer 11 and *via* a divider 19 to the clock inputs of the block decoding arrangements 12 to 15. In the demultiplexer 11 four symbols are inserted with the aid of the 672 MHz clock signal, which symbols are thereafter entered in parallel, with the aid of a clock signal having a frequency of 1/4 x 672 = 168 MHz, into the four parallel block decoding arrangements 12 to 15. Thereafter, using the 672 MHz clock signal four new symbols are inserted, which symbols are thereafter entered in parallel with the aid of the 168 MHz clock signal into the four parallel block decoding arrangements 12 to 15, etc. The four possible phase positions of the decoder write clock (168 MHz) relative to the shift clock (672 MHz) and the digital signal streams produced at the four parallel outputs of the demultiplexer are shown relative to each other in the time-sequence diagrams of Figure 3. In the time-sequence diagram of Figure 3a, the four word synchronizing characteristics K(1) ... K(4), and also the synchronizing characteristics K(10) ... K(40) are mutually in-phase. This implies that the demultiplexer 11 and demultiplexer 6 are in synchronism with each other. The respective digital input signal streams A, B, C and D of the transmission system are available again at the outputs 44 to 47 of the block encoding arrangements.

From the time-sequence diagrams shown in Figures 3b, 3c and 3d it will be obvious that the three other phase positions result in a different phase pattern in the word synchronizing characteristics K(1) ... K(4). The phase difference between the word synchronizing characteristics is not equal to 0 degrees, as it is at the transmitter side I of the transmission system. In all these three cases the demultiplexer 11 and the multiplexer 6 are not mutually in synchronism.

In the time-sequence diagram of Figure 3b the synchronizing characteristics K(1) and K(10) have a time lead relative to the other synchroniaing characteristics K(2) to K(4) and K(20) to K(40), respectively. In the time-sequence diagram of Figure 3c the synchronizing characteris-

tics K(1) and K(2) lead the synchronizing characteristics K(3) and K(4). The synchronizing characteristics K(10) and K(20) likewise have a time lead relative to the characteristics K(30) and K(40). In the time-sequence diagram of Figure 3d the synchronizing characteristic K(4) has a time lag relative to the other characteristics K(1) to K(3). The characteristic K(40) likewise lags the other characteristics K(10) to K(30).

The phase positions as shown in the Figures 3b to 3d are detected by means of the phase comparator arrangement 16, whereafter a control signal is applied to the divide-by-4 divider 15 for establishing synchronization between the multiplexer 6 and the demultiplexer 11. When the phase comparator 16 detects a phase position as shown in Figure 3a, the original digital signal streams A, B, C and D are then again available in the appropriate sequence at the outputs 44 to 47) of the block decoding arrangements 12 to 15 and no control voltage is applied to the divide-by-4 divider 19.

When the phase comparator 16 detects a phase position as shown in Figure 3b, the divide-by-4 divider 19 will operate once only as a divide-by-3 divider with the aid of the control signal produced by the phase comparator 16. This is shown in greater detail in Figure 4b. S(2) denotes the content of the demultiplexer 11 at the instant at which it is read in parallel. If now, in response to the control signal produced by the phase comparator 16, the divide-by-4 divider produces a write pulse once after three clock pulses which correspond to the symbols d2,c2,b2, the content of the demultiplexer 11 will be equal to S(20) after the next four clock pulses. The symbols a3, b3, c3 and d3 are now stored in the appropriate memory locations at the instant at which they are read in parallel, see Figure 3b. The demultiplexer 11 is now in synchronism with the multiplexer 6. The original digital signal streams A, B, C and D are then agains available in the appropriate sequence at the outputs 44 to 47 of the block decoding arrangements 12 to 15.

When the phase comparator detects a phase position as shown in Figure 3c, the divide-by-4 divider 19 will operate once as a divide-by-2 divider with the aid of the control signal produced by the phase comparator 16. This is shown in greater detail in Figure 4c. S(3) denotes the content of the demultiplexer 11 at the instant at which it is read in parallel. If now, with the aid of the control signal produced by the phase comparator 16 the divide-by-4 divider produces a write pulse once after two clock pulses which correspond to the symbols d2 and c2, the content of the demultiplexer 11 will be equal to S(30) after the next four clock pulses. The symbols a3, b3, c3 and d3 are now stored in the appropriate memory locations of the multiplexer 11, at the instant at which they are read in parallel, see Figure 3c. The demultiplexer 11 is now in synchronism with the multiplexer 6. The original digital signal streams A, B, C and D are then again available in the appropriate sequence at the outputs 44 to 47 of the block decoding arrangements 12 to 15.

When the phase comparator 16 detects a phase position as shown in Figure 3d, the divide-by-4 divider 19 will operate once as a divide-by-1 divider with the aid of the control signal produced by the phase comparator 16. This is shown in greater detail in Figure 4d S(4) denotes the content of the demultiplexer 11 at the instant at which it is read in parallel. If now, with the aid of the control signal produced by the phase comparator 16 produces a write pulse once after one clock pulse which corresponds to the symbol d2, the content of the demultiplexer 11 will be equal to S(40) after the next four clock pulses. The symbols a3, b3, c3 and d3 are now stored in the appropriate memory locations of the multiplexer 11 at the instant at which they are read in parallel. The demultiplexer 11 is now in synchronism with the multiplexer 6. The original digital signal streams A, B, C and D are then again available in the appropriate sequence at the outputs 44 to 47 of the block decoding arrangements 12 to 15.

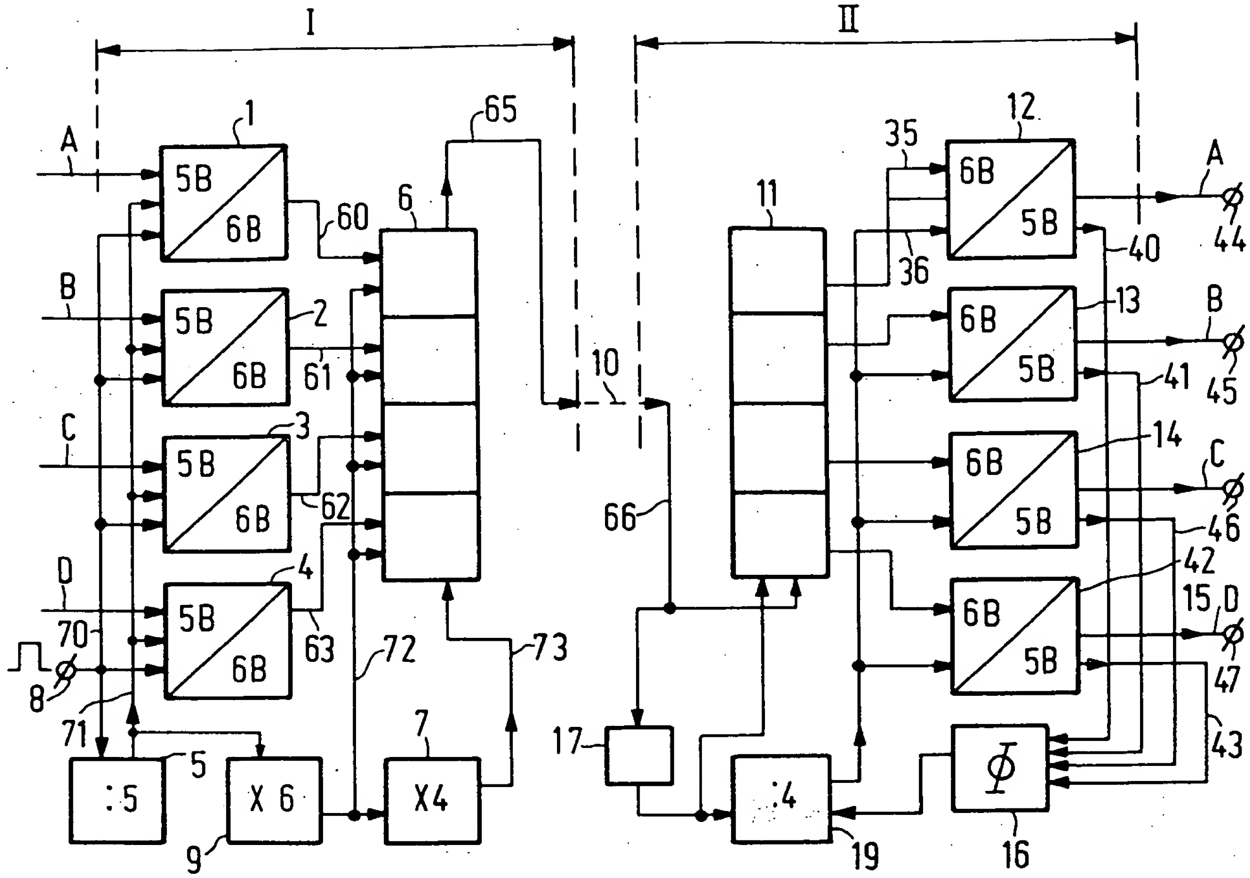
During the synchronizing phase the word synchro-

nization in the block decoding arrangement is temporarily lost. The word synchronization is not restored until the symbols a to d, reference 6, have passed the input of the demultiplexer 11.

Because of the fact that the block coding arrangements 1 to 4 and the block decoding arrangements 12 to 15 are operated at an N times lower symbol rate it is possible to integrate said arrangements, in spite of the high line symbol rate of the transmission system. In addition the described multiplexing method renders it possible to have all the signal processing operations, such as scrambling, justifying, line-coding, error-monitoring and word synchronization effected at an N times lower symbol rate. The multiplexer 6 and the demultiplexer 11 can be realized with the aid of a simple parallel/series converter and a simple series/parallel converter. It is also not necessary to add frame words and prolonged frame synchronization techniques.

Figure 5 shows an embodiment of a block decoding arrangement. It comprises an input shift register 30, a buffer 31, a decoder unit 32, an output shift register 33 and a word synchronizer 34. With the aid of the 168 MHz clock signal present at the clock input 36 a word having 6 binary symbols is written into the series register 30 via the input 35; see, for example, Figure 3a the word $a_1 \ldots a_6$. The word synchronizer 34 produces, after detection of the synchronization characteristic K(40), a pulse in response to which the content of the series register 30 is transferred to the buffer 31. Said word synchronizing characteristic is also applied to an input of the phase comparator 16 via the line 40. Using the decoder unit 32, the word having 6 binary symbols is converted into a word having 5 binary symbols which is applied in parallel to the output register 33. This output register is read with the aid of the 140 MHz clock signal present at the clock input 37. The original digital signal stream is available again at the output 44.

1. A higher order digital transmission system including a multiplexer having N parallel inputs and a digital demultiplexer having N parallel outputs for transmitting N mutually synchronized digital signal streams through a common digital path between said multiplexer and said demultiplexer, where N $\geqslant$ 2 and the multiplexer being arranged for cyclically and symbol-sequentially interleaving the digital signal streams to form a composite digital signal stream, the transmission system including at least a block encoding arrangement and at least a block decoding arrangement, characterized in that each of the N digital signal streams is applied to one of the parallel inputs of the multiplexer <u>via</u> a block encoding arrangement, that the N digital signal streams are entered synchronously into the block encoding arrangements under the control of a common clock signal and, in the respective block encoding arrangements are provided with a word synchronizing characteristic, that the parallel outputs of the demultiplexer are each connected to the input of a block decoding arrangement; that the signals applied to the parallel output of the demultiplexer are entered into the respective block decoding arrangements under the control of the clock signal recovered from the composite digital signal, that the outputs of the block decoding arrangements are each connected to a signal output of a transmission system, that in a phase comparator arrangement the word synchronizing characteristics of the block decoding arrangements are compared with each other, whereafter as a function of the phase differences measured between said word synchronizing characteristics the phase of the read clock is controlled such that thereafter the block decoding arrangments display the word synchronizing characteristics with the mutual phase differences produced at the transmitter end.


I
II
A
B
C
D
5B
6B
6B
5B
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
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19
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:5
X 6
X4
:4
Φ

FIG.1

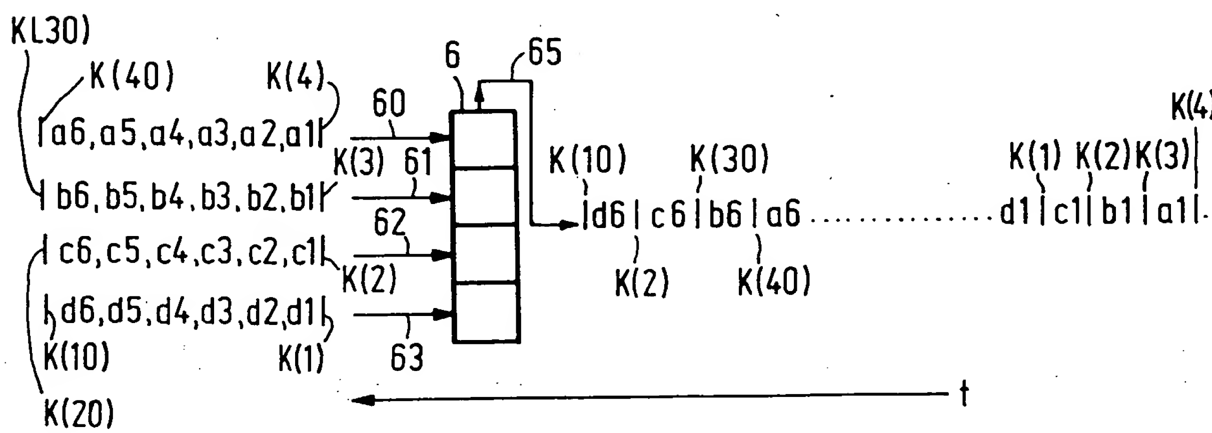
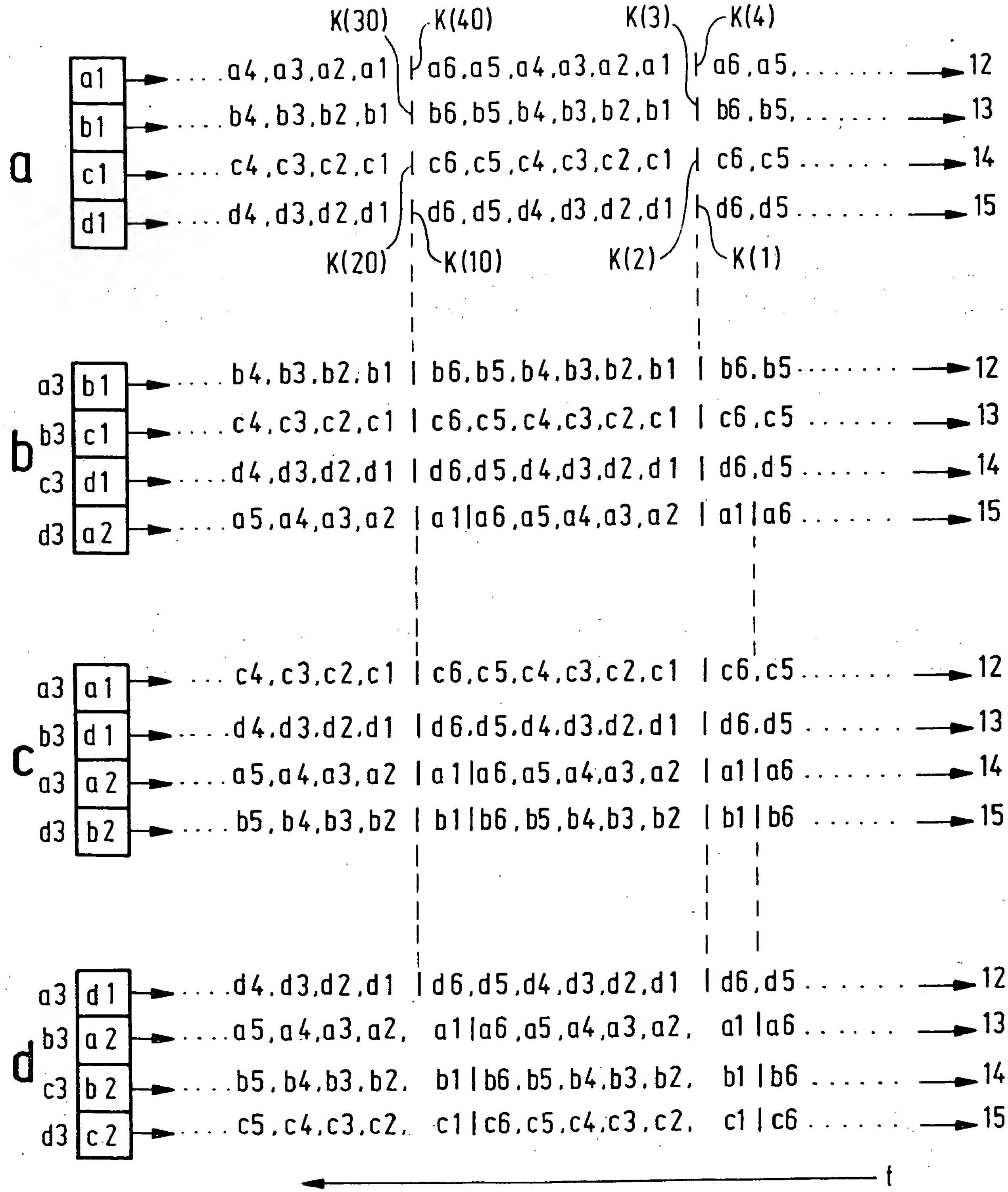

KL30)
K(40)
K(4)
a6,a5,a4,a3,a2,a1
K(3)
b6,b5,b4,b3,b2,b1
c6,c5,c4,c3,c2,c1
K(2)
d6,d5,d4,d3,d2,d1
K(10)
K(1)
K(20)
6
65
60
61
62
63
K(10)
K(30)
d6 | c6 | b6 | a6 .... d1 | c1 | b1 | a1
K(2)
K(40)
K(1) K(2) K(3)
K(4)
t

FIG.2



K(30)
K(40)
K(3)
K(4)
a
a1
b1
c1
d1
a4,a3,a2,a1 | a6,a5,a4,a3,a2,a1 | a6,a5, → 12
b4,b3,b2,b1 | b6,b5,b4,b3,b2,b1 | b6,b5, → 13
c4,c3,c2,c1 | c6,c5,c4,c3,c2,c1 | c6,c5 → 14
d4,d3,d2,d1 | d6,d5,d4,d3,d2,d1 | d6,d5 → 15
K(20)
K(10)
K(2)
K(1)
b
a3
b3
c3
d3
b1
c1
d1
a2
b4,b3,b2,b1 | b6,b5,b4,b3,b2,b1 | b6,b5 → 12
c4,c3,c2,c1 | c6,c5,c4,c3,c2,c1 | c6,c5 → 13
d4,d3,d2,d1 | d6,d5,d4,d3,d2,d1 | d6,d5 → 14
a5,a4,a3,a2 | a1 | a6,a5,a4,a3,a2 | a1 | a6 → 15
c
a3
b3
a3
d3
a1
d1
a2
b2
c4,c3,c2,c1 | c6,c5,c4,c3,c2,c1 | c6,c5 → 12
d4,d3,d2,d1 | d6,d5,d4,d3,d2,d1 | d6,d5 → 13
a5,a4,a3,a2 | a1 | a6,a5,a4,a3,a2 | a1 | a6 → 14
b5,b4,b3,b2 | b1 | b6,b5,b4,b3,b2 | b1 | b6 → 15
d
a3
b3
c3
d3
d1
a2
b2
c2
d4,d3,d2,d1 | d6,d5,d4,d3,d2,d1 | d6,d5 → 12
a5,a4,a3,a2, a1 | a6,a5,a4,a3,a2, a1 | a6 → 13
b5,b4,b3,b2, b1 | b6,b5,b4,b3,b2, b1 | b6 → 14
c5,c4,c3,c2, c1 | c6,c5,c4,c3,c2, c1 | c6 → 15
t

FIG.3

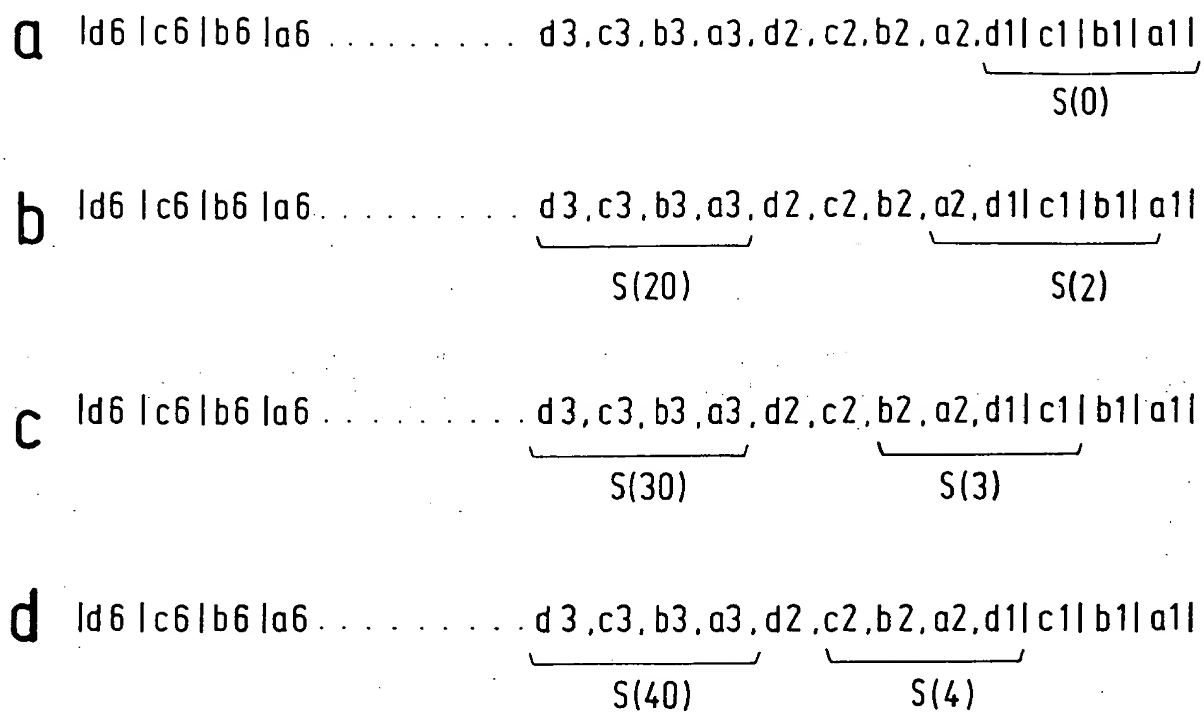
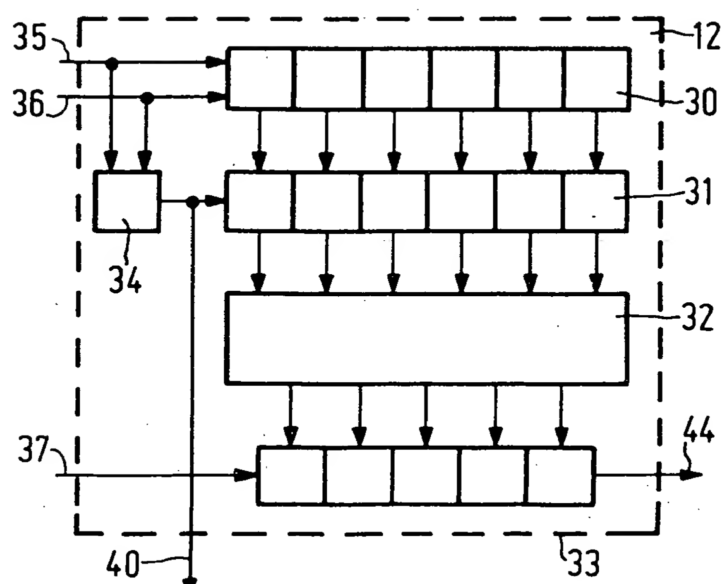

a |d6 |c6 |b6 |a6 .... d3, c3, b3, a3, d2, c2, b2, a2, d1| c1 | b1 | a1 |
S(0)
b |d6 |c6 |b6 |a6 .... d3, c3, b3, a3, d2, c2, b2, a2, d1| c1 | b1 | a1 |
S(20)
S(2)
c |d6 |c6 |b6 |a6 .... d3, c3, b3, a3, d2, c2, b2, a2, d1| c1 | b1 | a1 |
S(30)
S(3)
d |d6 |c6 |b6 |a6 .... d3, c3, b3, a3, d2, c2, b2, a2, d1| c1 | b1 | a1 |
S(40)
S(4)

FIG.4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12
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40
33

FIG.5

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EUROPEAN SEARCH REPORT

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EP 86 20 1034

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl 4)
Y	ELECTRICAL COMMUNICATION, vol. 57, no. 3, 1982, pages 251-258, Heidenheim, DE; A. BARBETTA et al.: "Digital multiplexers for rates from 2 to 565 Mbits-1 * Page 257, left-hand column, lines 11-15 * ---	1	H 04 J 3/04 H 04 J 3/06
Y	EP-A-0 040 351 (SIEMENS) * Page 4, line 12 - page 5, line 27; page 6, line 4 - page 7, line 8 * ---	1	
A	NACHRICHTENTECHNISCHE ZEITSCHRIFT NTZ, vol. 36, no. 1, January 1983, pages 16-21, Berlijn, DE; H. HOFMEISTER: "Digitaler multiplexer für vier plesiochrone 140-Mbit/s-digitalsignale" * Page 18, left-hand column, line 57 - page 19, centre column, last line * ---	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 04 J
A	IEE PROCEEDINGS, vol. 132, Pts. E and I, no. 2, March/April 1985, pages 68-72, Old Woking, Surrey, GB; I.C. WOOD et al.: "Design techniques for a 565/680 Mbit/s coder/decoder" * Page 68, left-hand column, line 1 - page 68, right-hand column, line 7 * --- -/-	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17-09-1986	VERSLYPE J.P.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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EUROPEAN SEARCH REPORT

0 206 409

EP 86 20 1034

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	CCITT Livre Jaune, Tôme III - Fascicule III 3. Reseaux numériques. Systèmes de transmission et équipement de multiplexage Avis G701-G941, VII Assemblée Plénière 10th-21st November 1980, Genève, CH * Page 223, annexe A *	1	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-14, no. 5, October 1979, pages 812-817, New York, US; J.B. HUGHES et al.: "A versatile ECL multiplexer IC for the Gbit/s range" * Page 814, left-hand column, lines 5-14 *	1	
A	EP-A-0 088 432 (NIPPON ELECTRIC CO.) * Page 3, line 7 - page 4, line 5 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17-09-1986	VERSLYPE J.P.

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X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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